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10/575,492	04/12/2006	Shinji Maekawa	740756-2947	3788

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EXAMINER	
ISAAC, STANETTA D	

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2812	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/575,492	MAEKAWA ET AL.	
	Examiner	Art Unit	
	STANETTA D. ISAAC	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16,17,19,20,24,26,27,36,37 and 39-46* is/are allowed.

6)☒ Claim(s) *1-9,11-15,18,21,23-25,29-35 and 38* is/are rejected.

7)☒ Claim(s) *10,27 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 4/07/08. Currently, claims 1-47 are pending.

Claim Objections

Claim 1 is objected to because of the following informalities: In line 4, "a liquid-repellent region" should read as "the liquid repellent region". Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-9, 11-15, 18, 21, 23-25, 29-35 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al (US PGPub.2003/0083203, hereinafter referred to as

"Hoshimoto") in view of Kimura et al (US PGPub 2004/0142544, hereinafter referred to as "Kimura").

Hashimoto discloses the semiconductor method as claimed. See figures 1-13, and corresponding text, where Hashimoto shows, pertaining to claim 1, a method for forming a wiring comprising the steps of: performing a liquid-repellent treatment on a surface ([0087] and [0097-0098]); performing selectively a lyophilic treatment on a region of the surface ([0100]); and forming a wiring on the lyophilic region by dropping a composition including a conductive material ([0102]).

Hashimoto shows, pertaining to claim 2, a method for forming a wiring comprising the steps of: forming a liquid-repellent region on a surface ([0087] and [0097-0098]); forming selectively a lyophilic region in the liquid-repellent region ([0100]); and forming the wiring on the lyophilic region by dropping a composition including a conductive material ([0102]).

Hashimoto shows, pertaining to claim 3, a method for forming a wiring comprising the steps of: forming a liquid-repellent region on a surface by a plasma treatment([0087] and [0097-0098]); forming selectively a lyophilic region in the liquid-repellent region ([0100]); and forming the wiring on the lyophilic region by dropping a composition including a conductive material ([0102]).

Hashimoto shows, pertaining to claim 6, wherein the lyophilic region is selectively formed by irradiating the liquid-repellent region with laser light ([0100]).

Hashimoto shows, pertaining to claim 7, wherein a region that is less liquid-repellent than the liquid-repellent region is formed as the lyophilic region ([0100]).

Hashimoto shows, pertaining to claim 8, wherein the composition is dropped by an ink-jetting method ([0106]).

Hashimoto shows, pertaining to claim 9, a method for forming a wiring comprising the steps of: forming a liquid-repellent region by forming a film containing fluorine on a surface ([0087] and [0097-0098]); forming selectively a lyophilic region in the liquid-repellent region([0100]); and forming the wiring on the lyophilic region by dropping a composition including a conductive material([0102]).

Hashimoto shows, pertaining to claim 11, wherein the lyophilic region is selectively formed by irradiating the liquid-repellent region with laser light ([0100]).

Hashimoto shows, pertaining to claim 12, wherein a region that is less liquid-repellent than the liquid-repellent region is formed as the lyophilic region ([0100]).

Hashimoto shows, pertaining to claim 13, wherein the composition is dropped by an ink-jetting method ([0106]).

Hashimoto shows pertaining to claim 14, a method for manufacturing a thin film transistor comprising the steps of: performing a liquid-repellent treatment on a surface ([0087] and [0097-0098]); performing selectively a lyophilic treatment on a region of the surface ([0100]); and forming a conductive film on the lyophilic treatment by dropping a composition including a conductive material ([0102]).

Hashimoto shows, pertaining to claim 15, a method for manufacturing a thin film transistor comprising the steps of: forming a liquid-repellent region on a surface ([0087] and [0097-0098]); forming selectively a lyophilic region in the liquid-repellent region ([0100]), and

forming the conductive film on the lyophilic region by dropping a composition including a conductive material ([0102]).

Hashimoto shows, pertaining to claim 18, a method of manufacturing a thin film transistor, comprising the steps of: forming a first liquid-repellent region by a plasma treatment on a surface for forming a gate electrode in an upper portion of the semiconductor film; forming selectively a first lyophilic regon in the first liquid-repellent region; and forming conductive film in the first lyophilic region of the surface of the semiconductor film dropping a composition including a conductive material.

Hashimoto shows, pertaining to claim 21, wherein the liquid-repellent region is formed by forming a CF.sub.2 bond on the surface by the plasma treatment ([0087] and [0097-0098]).

Hashimoto shows, pertaining to claim 23, wherein the liquid-repellent region is irradiated with laser light to selectively form the lyophilic region ([0100]).

Hashimoto shows, pertaining to claim 24, wherein the composition is dropped by an ink-jetting method ([0102]).

Hashimoto shows, pertaining to claim 25, a method for manufacturing a thin film transistor, comprising the steps of: forming a film containing fluorine ([0087] and [0097-0098]); forming selectively a first lyophilic region in the film containing fluorine ([0100]); forming a gate electrode on the lyophilic region by dropping a composition including a conductive material ([0102]); and performing a heat treatment for baking the gate electrode, and removing the film containing fluorine by the heat treatment ([0100]).

Hashimoto shows, pertaining to claim 29, wherein the liquid-repellent region is irradiated with laser light to selectively form the lyophilic region ([0100]).

Hashimoto shows, pertaining to claim 30, wherein the composition is dropped by an ink-jetting method ([0102]).

Hashimoto shows, pertaining to claim 31, a droplet discharging method, comprising the steps of: forming a lyophilic region by irradiating selectively on an object to be treated in which a liquid-repellent region is formed with light by a light irradiation unit([0087] and [0097-0098]; ([0100])); and discharging a droplet onto the lyophilic region by a droplet discharging unit, in a treatment chamber including the droplet discharging unit and the light irradiation unit ([0102]).

Hashimoto shows, pertaining to claim 32, a droplet discharging method, using a treatment apparatus in which a first treatment chamber having a plasma unit and a dielectric, and a second treatment chamber having a droplet discharging unit and a light irradiation unit, comprising the steps of: forming a liquid-repellent region in an object to be treated by the plasma unit and the dielectric in the first treatment chamber ([0087] and [0097-0098]); transporting the object to be treated into the second treatment chamber without being exposed to the atmosphere; forming selectively a lyophilic region in the object to be treated in which a liquid-repellent region is formed by the light irradiation unit in the second treatment chamber ([0100]); and discharging a droplet onto the lyophilic region by the droplet discharging unit ([0102]).

Hashimoto shows, pertaining to claim 33, wherein the droplet discharging unit and the light irradiation unit are integrally formed ([0115]).

Hashimoto shows, pertaining to claim 34, wherein the light irradiation unit includes laser light ([0115}).

Hashimoto shows, pertaining to claim 35, wherein the composition is dropped by an ink-jetting method ([0102]).

However, Hashimoto fails to show, pertaining to claims 1, 2, 3, 9, 14, 15, 18 and 25, forming selectively a (first) lyophilic region in the liquid-repellent region so that the surface includes the lyophilic region and the liquid-repellent region. In addition, Hashimoto fails to show, pertaining to claim 4, wherein the plasma treatment is performed at a pressure of 100 Torr to 1000 Torr. Finally, Hashimoto fails to show, pertaining to claim 18, forming a source electrode, drain electrode and gate electrode. Hashimoto fails to show, pertaining to claim 38, wherein the first liquid-repellent region is formed by forming a CF_2 bond on the surface by plasma treatment.

Hashimoto teaches performing a plasma treatment to create a liquid repellent ([0097-0098]).

Kimura teaches, pertaining to claims 1, 2, 3, 9, 14, 15 and 18, using laser irradiation to heat specific regions of the semiconductor film forming irradiated and non-irradiated regions, creating TFTs for driving circuits with faster switching characteristics, and TFTs for pixels that withstand high voltage (see figures 1B and 1C; [0038-0039]). In addition, Kimura teaches pertaining to claim 18, manufacturing thin film transistors that conventionally include a source electrode, drain electrode and gate electrode (figure 1E; [0046]).

1. It would have been obvious to one of ordinary skill in the art at the time of the invention to selectively form a (first) lyophilic region in the liquid-repellent region so that the surface includes the lyophilic region and the liquid-repellent region, in the method of Hashimoto, for its benefits of heating specific regions, as disclosed by the Kimura. The substitution of heating specific regions would be within the skill of one of ordinary skill in the art with the motivation of forming a strong attraction at the surface of the semiconductor film creating a smoothly

uniformed crystalline surface that provides faster switching characteristics at the irradiated portions and at the non-irradiated portions an ability to withstand high voltages. Also, regarding the plasma treatment being performed at a pressure of 100 Torr to 1000 Torr, pressure are parameters of optimization (*See In re Aller, Lancey and Hall* (10 USPQ 233-237)) where one of ordinary skill in the art would be capable of producing the desired parameters based on routine experimentation, for the purpose of creating a liquid repellent region. Forming a source electrode, drain electrode and gate electrode, in the method of Hashimoto, as taught by both Hashimoto in view of Kimura, would be obvious since both references teach forming integrated circuits known in the art where thin-film transistors would not be precluded as a known device that conventionally incorporate source electrode, drain electrode and gate electrodes to form the device. Finally, forming a liquid-repellent region by forming a CF_2 bond on the surface by plasma treatment would be obvious based on the teachings of Hashimoto performing the plasma treatment on the surface to create the liquid-repellent surface by using a fluorine based gas, such as, tetrafluoromethane (CF_4).

Allowable Subject Matter

2. Claims 10, 22, 27 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

3. Claims 16, 17, 19, 20, 26, and 36-47 are allowed over the prior art of record (subjected to further consideration and/or search).

4. The following is an examiner's statement of reasons for allowance:

5. The closest prior art of record, Hashimoto et al., US Patent Application Publication US 2003/0083203 and Kobayashi US Patent Application Publication US 2005/0040759, fails to show, the following steps of:

6. Pertaining to independent claim 16, "forming a second liquid-repellent region by a plasma treatment on a surface for forming a source electrode and drain electrode; forming selectively a second lyophilic region in the second liquid repellent region;"

7. Pertaining to independent claim 17, "forming a second liquid-repellent region by plasma treatment on the semiconductor film having one conductivity and gate insulating film; forming selectively a second lyophilic region in the second liquid repellent region;"

8. Pertaining to independent claim 19, "forming a second liquid-repellent region by performing a plasma treatment on the gate insulating film; forming selectively a second lyophilic in the second repellent region;"

9. Pertaining to independent claim 20, "forming a second liquid-repellent region by plasma treatment on the semiconductor film; forming selectively a second lyophilic region in the second repellent region;"

10. Pertaining to independent claim 26,"forming a second film containing fluorine over the semiconductor film having one conductivity and the gate insulating film; forming selectively a second lyophilic region in the second film containing fluorine;"

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

11. Applicant's arguments with respect to claims 1, 5-7, 11-23, 25-31, 34 and 35 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STANETTA D. ISAAC whose telephone number is (571)272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stanetta Isaac
Patent Examiner
October 29, 2008

/Alexander G. Ghyka/
Primary Examiner, Art Unit 2812